R20 Regulation *Subject code: 3E7DA*

TKR COLLEGE OF ENGINEERING AND TECHNOLOGY

(Autonomous, Accredited by NAAC with 'A+' Grade)

B.Tech VII Semester Supplementary Examinations, May 2026

ANALOG IC DESIGN

(ECE)

Maximum Marks: 70 Date: 14.05.2026 Duration: 3 hours

Note: **1.This question paper contains two parts A and B.**
2. Part A is compulsory which carries 20 marks. Answer all questions in Part A.
3. Part B consists of 5 Units. Answer any one full question from each unit.
4. Each question carries 10 marks and may have a, b, c, d as sub questions.

Part-A

All the following questions carry equal marks (10X2M=20 Marks)		Marks	CO	BTL
1	List the advantages of MOSFET.	2M	1	L1
2	Write the conditions of MOS transistor to operate in saturation and non-saturation regions.	2M	1	L1
3	Differentiate between voltage source and current source.	2M	2	L1
4	Define sensitivity of a voltage reference.	2M	2	L1
5	Define CMRR.	2M	3	L1
6	Draw the circuit of single ended input current amplifier.	2M	3	L1
7	Define amplifier.	2M	4	L1
8	Define operational amplifiers.	2M	4	L1
9	Write about ideal comparator.	2M	5	L1
10	What is clamped comparator?	2M	5	L1

Part-B

Answer All the following questions. (5X10M=50Marks)		Marks	CO	BTL
11	Explain the various components of large and small signal model of a MOS Transistor.	10M	1	L2
	OR			
12	With the help of required expressions explain Sub-threshold MOS Model.	10M	1	L2
13	Explain current sinks and sources with diagrams and list their characteristics.	10M	2	L2
	OR			
14	Explain in detail about Current and Voltage References.	10M	2	L2
15	Explain and draw the operation of high gain amplifiers architectures.	10M	3	L2
	OR			
16	Explain the operation of active load inverter and obtain small signal output resistance.	10M	3	L2

17	Explain about the design of CMOS op amps with necessary parameters.	10M	4	L2
	OR			
18	Explain the miller compensation in two stage op-amps.	10M	4	L2
19	Explain the design of a comparator with diagram and necessary equations.	10M	5	L2
	OR			
20	Explain the auto zeroing concept of improving the performance of a comparator.	10M	5	L2